REMARKS

In the Non-Final Office Action dated September 14, 2007, the Examiner: 1) rejected claims 10-27 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 7,024,596 ("*Xin*"); and 2) rejected claims 1-10 and 28 under 35 U.S.C. § 103(a) as being obvious over *Xin* in view of U.S. Pat. Pub. No. 2002/0087923 A1 ("*Eroz*").

With this response, Applicants amend claims 10, 17, 20 and 23. Based on the amendments and arguments contained herein, Applicants respectfully request reconsideration and allowance of the pending claims.

THE CITED REFERENCES

Xin teaches a RAM-based interleaver/de-interleaver technique that operates "code word by code word". *Xin's* interleaving/de-interleaving is based on a starting address register set with constant values and an offset register set with changing values (see Fig. 7A and 7B; col. 2, lines 51-58; and col. 10, line 65 – col. 11, line 16). *Xin* also discusses non-sequential delays lines during interleaving/de-interleaving which are related to memory addressing schemes (see Figs 2 and 3; col. 2, line 59 – col. 3, line 2; and col. 4, lines 19-33).

Eroz teaches a technique for interleaving blocks of indexed data of varying length by selecting an appropriately sized interleaver for a given block of indexed data (see paragraph [0010]). Once the interleaver is selected, the technique involves deleting (pruning) indexed data having an indices greater than the size of the interleaver (see paragraph [0049]).

§ 102 REJECTIONS

Claims 10-27 were rejected under 35 U.S.C. § 102(e) as being anticipated by *Xin*. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as

is contained in the...claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Amended claim 10, in part, requires "receiving a vector having multiple initial values, wherein the vector varies for different interleaving/de-interleaving techniques" and "selecting one of the initial values based on a cyclic pattern that varies for different interleaving/de-interleaving techniques." *Xin* does not teach these limitations. Instead, *Xin's* interleaving/de-interleaving technique involves a starting address register set with constant values (see col. 2, lines 54-56). Because *Xin's* starting values are constant, *Zin* does not teach "receiving a vector that varies for different interleaving/de-interleaving techniques" and "selecting an initial value from the vector based on a repeating pattern that varies for different interleaving/de-interleaving techniques" as in claim 10. For at least this reason, amended claim 10 and its dependent claims are not anticipated by *Xin* and are allowable.

Amended claim 17, in part, requires "the initial value is selected from a vector that varies for different interleaving/de-interleaving techniques compatible with the set of parameters." For much the same reasons, as described with respect to claim 10, *Xin* does not teach this limitation. Instead, *Xin's* starting values are constant and are limited to what is stored in the starting address register (see col. 2, lines 54-56). For at least this reason, amended claim 17 and its dependent claims are not anticipated by *Xin* and are allowable.

Amended claim 20, in part, requires "means for selecting an initial value from one of the parameters, the initial value is selected from a vector that varies for different interleaving/de-interleaving techniques compatible with the set of parameters". For much the same reasons, as described with respect to claim 10, *Xin* does not teach this limitation. *Xin's* starting values are constant and are limited to what is stored in the starting address register (see col. 2, lines 54-56). For at least this reason, amended claim 20 and its dependent claims are not anticipated by *Xin* and are allowable.

Amended claim 23, in part, requires "the interleaver/de-interleaver follows an initial value selection pattern that varies for different interleaving/de-interleaving

techniques compatible with the parameter values." For much the same reasons, as described with respect to claim 10, *Xin* does not teach this limitation. *Xin's* starting values are constant and are limited to what is stored in the starting address register (see col. 2, lines 54-56). *Xin* fails to teach an initial value selection pattern that varies for different interleaving/de-interleaving techniques as in claim 23. For at least these reasons, amended claim 23 and its dependent claims are not anticipated by *Xin* and are allowable.

§ 103 REJECTIONS

Claims 1-10 and 28 were rejected under 35 U.S.C. § 103(a) as being obvious over *Xin* in view of *Eroz*. "Any rejection under 35 U.S.C. § 103 must clearly and explicitly articulate the reason(s) why the claimed invention would have been obvious. MPEP § 2142. The framework for determining obviousness under 35 U.S.C. § 103 requires (1) determination of the scope and content of the prior art; (2) assessment of the differences between the claimed invention and the prior art; and (3) assessment of the level of ordinary skill in the pertinent art. *MPEP* § 2141 (citing *KSR International Co. v. Teleflex Inc.*, 550 U.S. ___, ___, 82 USPQ2d 1385, 1395-97 (2007)). Differences between the claim limitations and the prior art weighs in favor of non-obviousness. To establish obviousness, each of the claim limitations must be taught or suggested by the prior art. See *CFMT, Inc. v. YieldUp Int'l Corp.*, 349 F.3d 1333, 1342 (Fed. Cir. 2003). Applicants traverse the Examiner's obviousness rejection.

Claim 1, in part, requires "a controller coupled to the initial value selector, the offset selector, and the pruning adjuster, the controller asserts control signals provided to the initial value selector, the offset selector, and the pruning adjuster, such that a plurality of interleaving/de-interleaving algorithms are executable." *Xin* and *Eroz* are each directed to a particular algorithm and do not have a controller that enables execution of a plurality of interleaving/de-interleaving algorithms as in claim 1. Further, combining *Xin* and *Eroz* as suggested by the Examiner is improper. Not all interleavers/de-interleavers benefit from or require pruning as is suggested by the

Examiner. *Xin* teaches a RAM-based interleaver/de-interleaver technique that is based on a starting address register set with constant values and an offset register set with changing values (see Fig. 7A and 7B; col. 2, lines 51-58; and col. 10, line 65 – col. 11, line 16). *Xin's* interleaving/de-interleaving does not discuss pruning, but is still described as a "very efficient" technique that reduces register and memory requirements for interleaving/de-interleaving (see col. 2, lines 1-9 and 30-33). Adding *Eroz's* pruning capability to *Xin* appears to complicate *Xin's* already efficient operation and would render *Xin* unsatisfactory for its principle of operation which reduces hardware requirements such as registers and memory. MPEP § 2143.01, part V.

Furthermore, *Xin* does not discuss pruning as is recognized by the Examiner. Office Action dated 09/14/07, page 3. Thus, adding *Eroz's* pruning hardware is presumably unnecessary and would improperly modify *Xin's* principle of operation which does not appear to rely on pruning. MPEP § 2143.01, part VI. Again, not all interleavers/de-interleavers benefit from or require pruning. The Examiner has not addressed these issues and thus has not clearly articulated the reasons why Applicants' claim 1 would have been obvious in view of *Xin* and *Eroz* as is required. For at least these reasons, claim 1 and its dependent claims are allowable over *Xin* and *Eroz*.

CONCLUSIONS

In course of the foregoing discussions, Applicants may have at times referred to claim limitations in shorthand fashion, or may have focused on a particular claim element. This discussion should not be interpreted to mean that the other limitations can be ignored or dismissed. The claims must be viewed as a whole, and each limitation of the claims must be considered when determining the patentability of the claims. Moreover, it should be understood that there may be other distinctions between the claims and cited art which have yet to be raised, but which may be raised in the future.

Applicants respectfully request reconsideration and that a timely Notice of Allowance be issued in this case. In the event that an extension of time is necessary to allow for consideration of this paper, such extensions are hereby petitioned under

37 C.F.R. § 1.136(a), and any fees required (including fees for net addition of claims) are hereby authorized to be charged to Texas Instruments Incorporated's Deposit Account No. 20-0668 for such fees.

Respectfully submitted,

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